REMARKS

Claims 1-46 are pending. Claims 12-46 have been withdrawn from further consideration. Claim 1 has been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

In the Specification

The Abstract of the Disclosure and the Title of the Invention were objected to. Specifically, the Abstract was objected to for exceeding 250 words and the Title was objected to as allegedly being non-descriptive. Applicant has amended the Abstract and the Title in view of these objections. Accordingly, Applicants respectfully requests reconsideration and withdrawal of these objections.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 4, 5, and 11 were rejected under 35 U.S.C. § 102(a) over Kawashima (U.S. Patent No. 6,163,053). Applicant respectfully traverses this rejection.

Claim 1 recites, in part, a semiconductor device which includes a first, a second and a third impurity doped layer. The three impurity doped layers make up a multilayer lamination structure with two junctions therebetween. In contrast, Kawashima discloses a channel region 19, a well region 15 under the channel region 19, and an opposite polarity region 156 surrounded by the well region 15 (column 6, lines 15-25). Kawashima does not disclose that the three regions, 15, 19, and 156, make up a multilayer lamination structure with two junctions therebetween. In fact, Kawashima only teaches (Figures 6-9) that the region 156 is surrounded by the well region 15. Accordingly, Kawashima does not teach that the three impurity doped layers make up a multilayer lamination structure with two junctions therebetween, as recited in claim 1.

Claims 4, 5, and 11 are believed allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claim Rejections Under 35 U.S.C. § 103

A. Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) over Kawashima. Applicant respectfully traverses this rejection.

Claims 2 and 3 are believed allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

B. Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) over Kawashima in view of Cheek et al. (U.S. Patent No. 6,162,694). Applicant respectfully traverses this rejection.

Claims 9 and 10 are believed allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Conclusion

Applicant appreciates the Examiner's indication that claims 6-8 contain allowable subject matter and would be allowable if rewritten in independent form. However, in view of the foregoing, all the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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Enclosure: Appendix

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The Title of the Disclosure has been amended as follows:

SEMICONDUCTOR DEVICE [AND METHOD OF FABRICATING THE SAME] REALIZING CHARACTERISTICS LIKE A SOI MOSFET

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region;

a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said three impurity doped layers make up a multilayer lamination structure with two junctions therebetween, wherein

said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, and wherein

said second impurity doped layer is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers.

IN THE ABSTRACT OF THE DISCLOSURE:

The Abstract of the Disclosure has been amended as follows:

[A semiconductor device includes a semiconductor substrate, a gate electrode as formed over a surface of the substrate with a gate dielectric film interposed therebetween, source/drain layers formed in said semiconductor substrate to oppose each other with a channel region residing between these layers at a location beneath the gate electrode, the source/drain each having a low resistivity region and an extension region being formed to extend from this low resistivity region toward the channel region side and being lower in impurity concentration and shallower in depth than the low resistivity region,] In a semiconductor device, source/drain layers have a low resistivity region and an extension region extending from the low resistivity region toward the channel region. The extension regions are lower in impurity concentration and shallower in depth than the low resistivity regions. The device also has a first impurity-doped layer [of a first conductivity type] formed in the channel region between the source/drain layers, a second impurity-doped layer [of a second conductivity type] formed under the first impurity-doped layer, and a third impurity-doped layer [of the first conductivity type] formed under the second impurity-doped layer. [, wherein the] The first impurity-doped layer is equal or less in junction depth than the extension regions. [of the source/drain layers whereas the second impurity-doped layer is designed in] The second impurity doped layer has impurity concentration and thickness to be fully depleted due to a built-in potential as created between the first and third impurity-doped layers.

End of Appendix